Alleviating Electromigration Through Re-Engineering The Interface Between Cu & Dielectric-Diffusion-Barrier in 90 nm Cu/SiOC (k=2.9) Device

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Abstract

Despite the initial success in integrating 90 nm Cu/SiOC (k=2.9) device using the HSQ via-filler scheme, the reliability issues remain. By correlating EM with the moisture blocking capability of the dielectric-diffusion-barrier, we target the factors contributing to the moisture blockage, namely, the N and H-content within SiC. Consequently, increasing the N/H ratio in the SiCN film, we demonstrated a significant enhancement in EM reliability.

Introduction

With SiOC becoming one of the dominant choices for Cu/low-k in 90 nm design nodes, several attempts have recently surfaced to overcome the challenges involved in integrating Cu/SiOC, such as the resist poison, low etch selectivity, and crown fence [1-3]. Among these, the HSQ via-filler scheme [3] has shown promising results by resolving said issues while maintaining manufacturing simplicity. Despite the demonstrated feasibility in 90 nm Cu/low-k integration, the ideal candidate for the dielectric-diffusion-barrier, e.g., SiN, SiC, or SiCN, remains uncertain because of its processing differences [4-7]. Moreover, integrating low-k constantly poses reliability risks [8-10]. In this paper, we focus on improving the EM reliability through re-engineering the Cu/dielectric-diffusion-barrier interface.

Experimental Details

The 2-level dual damascene Cu interconnects were fabricated using 90nm process technology. In this process, the OSG(k=2.9) and HSQ were used for low-k dielectric and sacrificial layer to prevent PR poisoning. Trench and via were etched using reactive ion etching(RIE). A Hollow Cathode Magnetron PVD(HCM-PVD) Ta/TaN bilayer scheme was used for the barrier layer. A Cu seed layer was followed by Electro-Chemical Deposition(ECD) Cu. The overfilling Cu was polished off by Chemical Mechanical Polishing(CMP). For this study four different PE-CVD dielectric deposition processes were developed: (1) SiN films were deposited at 400 °C using silane, ammonia, and nitrogen, (2) SiC films were deposited at 400 °C using tetra-methylsilane (4MS) and helium (3) two kind of SiCN films were deposited at 400 °C using 4MS, helium, ammonia, and 4MS, ammonia, nitrogen (Table 1). SiC and SiCN films have a significantly lower dielectric constant than SiN. Chemical composition data of SiN, SiC, SiCN-1, and SiCN-2 films was collected using Rutherford Backscattering Spectrometry (RBS) and listed in Table 2. Electromigration kinetic studies were carried out on wafer-level in a temperature range from 280 to 300°C applying current densities between 1 and 2MA/cm^2. Failure criterion was 10% relative increase of resistance.

Results and Discussion

Contrary to the typical EM failures located around the via-bottom area for devices with SiN as the dielectric-diffusion-barrier (Fig. 1a), via-EM failures in devices with SiC initiate from the void growth along the Cu/SiC interface (Fig. 1b). In addition, the MTF matches that of the line-EM as shown in Fig. 2a, indicating the interfacial properties of Cu/SiC as the severest reliability-limiting factor even for via-containing modules. The calculated current density exponent, n, for the M1 line of 1.1 (Fig. 2b) corresponds to the failure mechanism by void growth rather than by nucleation, suggestive of the presence of defects that significantly curtails the energy barrier for void nucleation along the Cu/SiC interface prior to EM-stressing.

Inserting a SiN layer immediately adjacent to Cu, on the other hand, extends the failure time as shown in Fig. 3a. This slight improvement can be attributed to the more efficient oxygen blockage of SiN over SiC as shown in Fig. 3b, hindering the formation of CuO_X along the Cu/SiN interface. Figs. 3c and 3d further confirm through the stress change correlation the decidedly greater moisture, e.g., O_2, O^-, OH^-, H_2O, etc., penetration in SiC over SiN; SiC used in this particular study is processed via 4MS + He. One can, thus, deduce that the EM characteristics deteriorated per CuO_X formation along the Cu/SiC interface. Use of SiN, however, cannot serve as the remedy lest the capacitance increase and/or etch-selectivity diminish.

While not completely clear, one of the possible core differences between SiN and SiC may be correlated to the N and H content. Specifically, it is plausible that the relatively

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greater H-content in SiC accelerates the moisture movement in SiC [11] given the increase in number and/or size of pores with the amount of H in SiC; SiC used in this specific study contains approximately 43.4 % H in the form of Si-CH_X/Si-H_X while SiN comprises 21.3 % due to its non-porous nature(Table 2). The increase in the N-content in SiC, on the other hand, results in a greater probability of Si-N bonding that in turn reduces the number of pores, and, enhances the moisture-blocking strength.

To test this hypothesis (Fig. 4a), SiCN-1 and SiCN-2 films were produced by controlling the N and H-content along the Cu/dielectric-diffusion-barrier interface via NH_3 and N_2 as shown in Table 1. The first test entailing stress change measurement as a function of air exposure time (Fig. 4b) confirms the correlation between the moisture blockage characteristics and the N/H ratio in dielectric-diffusion-barrier films (Table 2). The order of improvement is "SiCN-2" ≅ SiN > "SiCN-1" > SiC in which the addition of N_2 (SiCN-2) on top of NH_3 (SiCN-1) has the effect of further diluting or reducing the amount of H, essentially increasing the N/H ratio. The line-EM tests also corroborate the effect as shown in Fig. 4c. Based on the experimentally determined activation energy of 1.0 eV, the lifetime is projected to exceed well over 10 years.

The significance of producing Cu/dielectric-diffusion-barrier interface of high quality is further supported through the test fortifying the presumed weakest point in via-EM failures, namely, the via-bottom regions. Certain processing instabilities can leave voids behind at the corner of via-bottom that later act as nuclei in via-EM failures. A barrier metal process that reinforces said weakest link by re-sputtering Ta from via-bottom to its adjacent sidewall/corner regions (Fig. 5a) somewhat extends the via-EM failure times, but still falls short of meeting the 10-yr lifetime guarantee in the case of SiC. Upon applying SiCN-2 processed with the enhanced moisture-blocking strength, the number of via-EM failure points drastically falls and the MTF also extends by one order of magnitude (Fig. 5b), easily exceeding the lifetime specification.

Conclusions

Despite the initial success in integrating Cu/SiOC (k=2.9) device in 90 nm design node, the reliability aspect requires further attention. The EM failure analyses point to the choice of dielectric-diffusion-barrier. By correlating EM with the moisture blocking capability of dielectric-diffusion-barrier, we target the factors contributing to the moisture blockage, namely, the N and H-content within SiC. Consequently, interface between Cu and dielectric-diffusion-barrier as the reliability limiting region instead of the corner of via-bottom. Engineering said interface, however, is a difficult task due to the wide range of inconsistencies reported regarding the ideal increasing the N/H ratio in the SiCN film, we demonstrated a significant enhancement in EM reliability in 90 nm Cu/SiOC (k=2.9) devices.

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Table 1. Film properties of four different dielectric-diffusion-barriers by controlling the N and H content

	SiN	SiC	SiCN-1	SiCN-2
Source Chemical	SiH_4+NH_3+N_2	4MS+He	4MS+He+NH_3	4MS+NH_3+N_2
Reflective Index	2.05	1.98	1.88	1.92
Stress (dyne/cm^2)	-2.51E+9	-1.05E+9	-1.47E+9	-1.69E+9
k-value	7.0	5.0	4.5	5.0

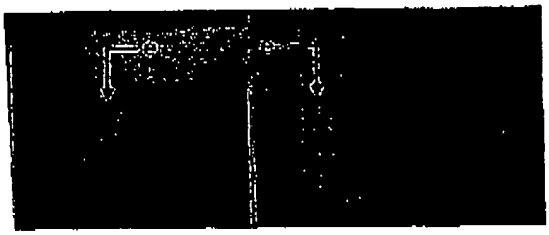


Fig. 1 Effect of using (a) SiN vs. (b) SiC as the dielectric-diffusion-barrier in terms of via-EM failure mode

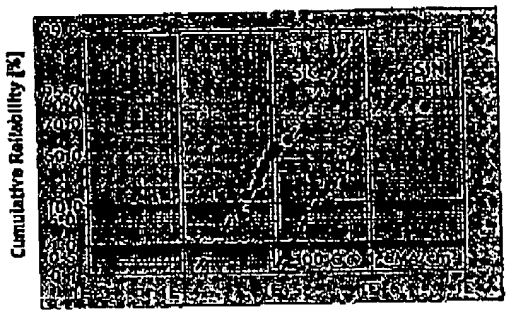


Fig. 3a. Failure distribution of line-EM for SiC vs. SiN

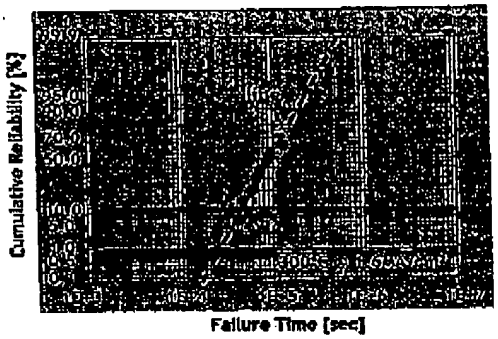


Fig. 2a. Statistical equivalence in the failure distributions of via- vs. line-EM for the SiC case.

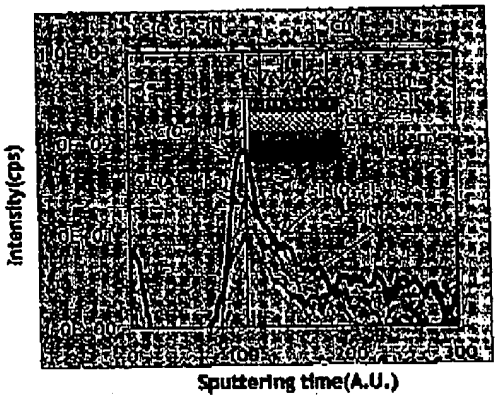


Fig. 3b. SIMS showing the CuO_x peak along the Cu/dielectric-diffusion-barrier interface before and after O_2 plasma treatment.

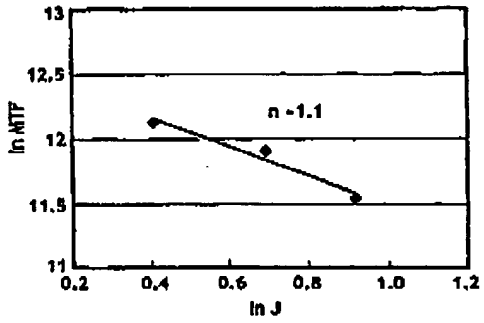
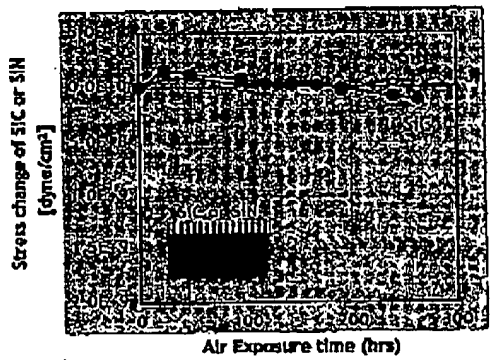
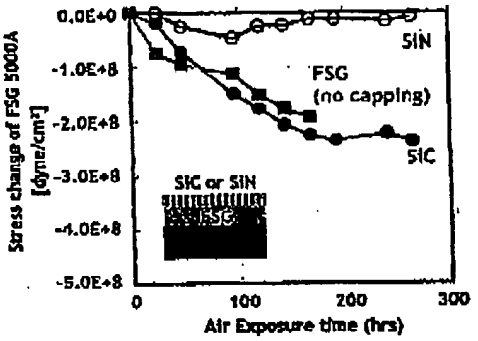


Fig. 2b. Current density exponent, n, for line-EM in the case of applying SiC as the dielectric-diffusion-barrier. The n-value of 1.1 suggests void growth as the dominant EM failure mode.



Figs. 3c. Stress change as a function of air exposure time for SiC/Si vs. SiN/Si stack.



Figs. 3d. Dielectric-diffusion-barrier capped oxide stress change with ambient exposure time

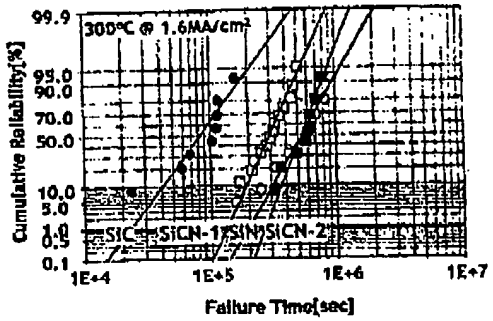


Fig. 4c. Failure distribution of line-EM for re-engineered Cu /dielectric-diffusion-barrier interfaces.

Fig. 4a. Schematic diagram depicting a model of moisture penetration in relation to N & H-content for SiN vs. SiC

Fig. 5a. TEM showing the fortified via-bottom regions through re-sputtered Ta from via-bottom onto via-sidewall.

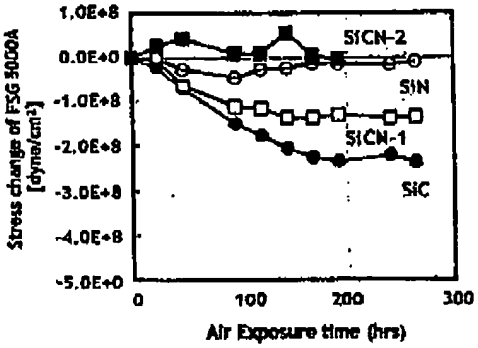


Fig. 4b. Stress change as a function of air exposure time for various re-engineered Cu/SiCN interfaces. Samples are of the same structure as that shown in Fig. 3d

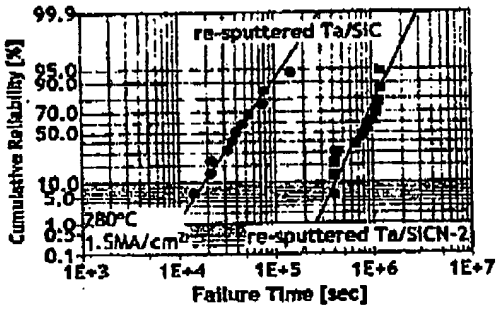


Fig. 5b. Failure distribution of via-EM in fortified via-bottom regions for conventional Cu/SiC vs. re-engineered Cu/SiCN-2 interface.

Table 2. Chemical composition of four different dielectric-diffusion-barriers by controlling the N and H content

	% Si	% C	% N	% H	*N/H ratio*
SiN	37.5	-	41.2	21.3	*1.9*
SiC	25.3	31.3	-	43.4	-
SiCN-1	25.5	19.9	17.1	37.5	*0.4*
SiCN-2	27.2	19.3	24.3	29.2	*0.8*